scribe a current normalization factor. Since past values of the alpha and beta recursions are available earlier, the normalization factor calculation time can be removed from the alpha and beta update circuit. The resulting increase in speed is significant. Hence, the normalization factor is actually an input to the alpha and beta circuit, as opposed to being computed within the circuit itself.

FIG. **12** illustrates an alternative embodiment of a circuit **48** for calculating the scale factor applied to the alpha and beta function values in the alpha and beta update circuit as the minimum of all probability function values input to the circuit. This embodiment of the normalizer **48** (scale factor calculator) comprises a plurality of circuits **150** that output the minimum of two input numbers. These are connected in a series of parallel stages to form a tree-like structure which calculates the minimum of all values input to the scale factor calculator. This minimum value is finally clocked out by a latch **154**.

The use of past alpha and beta recursion values of the recursions to prescribe current normalization factors presents an additional source of feedback in the alpha and beta recursions. To limit such feedback, the normalization is preferably only applied every V update cycles, where V is the number of cycles of the alpha (or beta) recursion needed for the normalization calculation, e.g., three. Advantageously, because of the way in which the state probability estimates are ultimately used in the turbo decoder, the periodic application of normalization does not cause any performance degradation therein.

While the preferred embodiments of the present invention have been shown and described herein, it will be obvious that such embodiments are provided by way of example only. Numerous variations, changes and substitutions will occur to those of skill in the art without departing from the invention herein. Accordingly, it is intended that the invention be limited only by the spirit and scope of the appended claims.

What is claimed is:

1. A turbo decoder comprising a plurality of component decoders for decoding component code words of turbo codes, each component decoder comprising:

circuits for receiving and storing received symbols corresponding to a turbo code word;

a gamma block for calculating substantially simultaneously for a plurality of decoder trellis stages a plurality of first and second gamma probability function values, which correspond to the branches of a component code's trellis, the gamma block receiving as inputs the received symbols' channel transition probabilities and a priori bit probabilities for the bits represented by the received symbols, which correspond to the decoder trellis stages;

an alpha block for receiving the gamma probability function values from the gamma block and for recursively calculating alpha probability function values, corresponding to a plurality of trellis state indices, substantially simultaneously by a plurality of circuits, the gamma function values for each alpha probability function value being selected via selection switches, the alpha block further receiving a plurality of alpha probability function values from the previous step of the recursive calculation, the alpha block further comprising circuits for scaling each resultant alpha probability function value substantially simultaneously by a scale factor which is provided as an input to the alpha block;

a beta block for receiving first gamma probability function values from the gamma block and for recursively calculating beta probability function values, corresponding to a plurality of trellis state indices, substantially simultaneously by a plurality of circuits, the gamma function values for each beta probability function value being selected via selection switches, the beta block further receiving a plurality of beta probability function values from the previous step of the recursive calculation, the beta block signal processing further comprising circuits to scale each resultant beta probability function value substantially simultaneously by a scale factor which is provided as an input to the beta block;

a sigma block for receiving the alpha and beta probability function values, respectively, from the alpha and beta blocks, respectively, receiving the second gamma probability function values from the gamma block and receiving a second set of alpha and beta probability function values, respectively, from alpha and beta memories, respectively, and for calculating substantially simultaneously for a plurality of decoder trellis stages a plurality of sigma probability function values which correspond to the branches of a component code's trellis at the trellis stages corresponding to the received symbols, which are being processed at that time, the sigma block also comprising a plurality of pipelined trees of summation functions of all sigma values belonging to each of two subsets of the sigma probability function values for each of the plurality of decoder trellis stages, one subset comprising the sigma function values for trellis branches labeled with a data bit value of zero and the other subset comprising the sigma function values for trellis branches labeled with a data bit value of one, the sigma block calculating the difference of the outputs of the two summation functions for each of the plurality of decoder trellis stages to produce the logarithm of the likelihood ratio of the maximum a posteriori decoded bit value probabilities for each of the plurality of trellis stages as outputs of the turbo decoder;

a plurality of memory cells for storing channel transition probabilities, received symbols, half of the alpha probability function values, half of the beta probability function values, a posteriori and a priori data bit log-likelihood ratios, and a de-interleaving pattern;

a circuit for calculating the negative of the logarithm of the probability that a decoded data bit value is zero from the log-likelihood ratio of data bit value probabilities;

a circuit for calculating the negative of the logarithm of the probability that a decoded data bit value is one from the log-likelihood ratio of data bit value probabilities;

a circuit for making decoded bit decisions from the corresponding log-likelihood ratio; and

a circuit for outputting decoded data bits.

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